WHAT IS CLAIMED IS:

1. A memory module, comprising:

an array of connections arranged in rows and columns such that there are first and second outer columns, and those connections in the first and second outer columns can be interchanged.

2. The memory module of claim 1, wherein the first outer column is a nearside column and the second outer column is a far-side column.

3. The memory module of claim 1, wherein there are third and fourth outer columns having interchangeable connections.

4. The memory module of claim 1, the memory module further comprising a package selected from the group comprised of: X16, and X4/X8.

5. A memory system, comprising:

a first memory module mounted on a first side of a substrate, the first memory module comprising:

an array of connections arranged in rows and columns such that there are first and second outer columns, and that connections in the first and second outer columns can be interchanged;

a second memory module mounted on a second side of the substrate, comprising:

an array of connections arranged in rows and columns such that there are first and second outer columns, and that connections in the first and second outer columns can be interchanged;

a memory controller to control interchange of signals between first and second outer columns of the memory modules;

signal traces in the substrate, wherein the connection in the first and second outer columns of the first and second memory modules are arranged such that signals routed on the traces have uniform routing lengths.

6. The memory system of claim 5, the substrate further comprising a multi-layered printed circuit board.

7. The memory system of claim 6, signal traces further comprising multiple signal traces in multiple layers of the printed circuit board.

8. The memory system of claim 5, the memory modules being packaged in a package selected from the group comprised of: X16 and X4/X8.

9. A memory device, comprising:

a memory array having an array of memory connections arranged in rows and columns;

a module to receive the memory array;

a connector on the module having an array of connector connections arranged in rows and columns, such that the memory connections and the connector connections can be interchanged.

10. The memory device of claim 9, the module further comprising a dual, in-line memory module.

11. The memory array of claim 10, the module being selected from the group comprised of: a X16 package, and an X4/X8 package.

12. A method of designing a memory device, comprising:

determining an interchangeable set of memory signals and a fixed set of memory signals;

arranging the interchangeable set of memory signals in outer columns of a connection array; and

arranging the fixed set of memory signals in inner columns of a connection array.

13. The method of claim 12, determining an interchangeable set of memory signals further comprising identifying address connections within a row as being interchangeable.

14. The method of claim 12, determining an interchangeable set of memory signals further comprising identifying bank address connections as being interchangeable.

15. The method of claim 12, arranging the interchangeable set of memory signals in outer column further comprising arranging the interchangeable set of memory signals in two outer columns on each side of the connection array.

16. The method of claim 12, arranging the interchangeable set of memory signals in outer column further comprising arranging the interchangeable set of memory signals in one outer column on each side of the connection array.